REMARKS

Claims 1, 3 and 6-8 are pending in the instant patent application. Claims 2, 4, 5 and 9-15 were previously canceled. Applicants respectfully request reconsideration of the instant application and pending Claims.

Examiner Interview

Applicants respectfully request an Examiner's Interview prior to the issuance of the next Office Action if the next Office Action includes a rejection that is again based on the Tanaka and Heim references discussed below.

103 Rejection

Claims 1, 3 and 6-8 are rejected under 35 U.S.C. 102 as being anticipated by Tanaka (US Patent No. 6,756,675; hereinafter "Tanaka") in view of Heim (US Patent No. 5,248,903). Applicants have reviewed the cited reference and respectfully submit that the embodiments of the claimed invention that are set forth in Claims 1, 3 and 6-8 are not anticipated or rendered obvious by Tanaka in view of Heim.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a semiconductor device. Claim 1 is reproduced in its entirety below for convenience of the Examiner.

> 1. A semiconductor device comprising:
> a pad metal layer having a perimeter area and a center area;
> a lower metal layer having a plurality of apertures below said center area of said pad metal layer, wherein said apertures are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures;
> an interlayer dielectric formed between said pad metal layer and said lower metal layer;
> a plurality of vias formed in said interlayer dielectric, wherein said plurality of vias electrically couple said pad metal layer and said lower

metal layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer; and

an insulating dielectric layer that covers said perimeter area of said pad metal layer.

Claims 3 and 6-8 depend from Claim 1 and recite additional limitations of the claimed invention.

Tanaka in view of Heim does not anticipate or render obvious the embodiments of the invention as set forth in Claims 1, 3, 6 and 8. Tanaka in view of Heim is deficient as Tanaka does not teach or suggest all of the limitations of the claimed embodiments and Heim does not remedy the deficiencies of Tanaka. In particular, Tanaka does not teach or suggest a semiconductor device that includes a plurality of vias formed in an interlayer dielectric that is formed between a pad metal layer and a lower metal layer that has apertures, "wherein said plurality of vias electrically couple said pad metal layer and said lower metal layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer" as is set forth in Claim 1. Furthermore, Heim does not teach or suggest modifying Tanaka to include these features to remedy the deficiencies of Tanaka. In fact, Heim does not teach or suggest these limitations at all.

Claim 1 has been amended to clarify the relationship between the vias located in the interlayer dielectric to the apertures located in the lower metal layer. Support for the newly added limitation can be found in Applicants' specification at page 4, lines 10-37. It

is important to note that the newly added limitations provide clarification that the vias are located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer. It should be appreciated that this limitation (along with the others recited in the Claims) must be taught or suggested by the cited reference in order for a proper prima facie case for rejection to be supported thereby. However, Applicants respectfully submit that the newly added limitation is not taught or suggested anywhere by Tanaka et al. If a rejection based on Tanaka et al. is maintained Applicant respectfully requests that the location in the references where the aforementioned limitation is taught or suggested be identified.

In contrast to the embodiment of the claimed invention set forth in Claim 1, Tanaka shows a dissimilar semiconductor device that features a triple layered device structure. Importantly, Tanaka discloses that conductive members (110a-110d), which are equated in the rejection to the recited vias of Claim 1, are located only underneath the four corner areas of electrode layer 100 (equated to the recited pad metal layer) shown in Figure 1. Referring to Figure 1, it is apparent that these conductive members are confined to the aforementioned corner areas and actually do not form a ring below electrode layer 100. This is very different from the embodiment of the invention that is set forth in Claim 1 which, as discussed, features recited vias that form a ring arrangement below an outermost perimeter of a pad metal layer.

Based on the aforementioned review of Tanaka, Applicants respectively submit that nowhere in the Tanaka reference is a semiconductor device that includes a plurality of vias formed in an interlayer dielectric that is formed between a pad metal layer and a lower metal layer that has apertures, "wherein said plurality of vias electrically couple

said pad metal layer and said lower metal layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer" as is set forth in Claim 1 taught or suggested. Consequently, as alluded to above, Tanaka fails to teach or suggest all of the limitations recited in Claim 1.

Heim does not teach or suggest a modification of Tanaka that that would remedy the deficiencies of Heim discussed above. In particular, Heim does not teach or suggest a semiconductor device that includes a plurality of vias formed in an interlayer dielectric that is formed between a pad metal layer and a lower metal layer that has apertures, "wherein said plurality of vias electrically couple said pad metal layer and said lower metal layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer" as is set forth in Claim 1.

In contrast, Heim shows a dissimilar bond pad scheme for semiconductor devices. The bond pad scheme disclosed by Heim is dissimilar from that which is embodied in the in the semiconductor device that is set forth in Claim 1 as the scheme disclosed by Heim does not include vias that are located below the outermost perimeter of a pad metal. It should be appreciated that in the instant rejection of Claims 1, 3 and 6-8, conductive layer 214 shown in Figure 2A of Heim is equated to the recited pad metal layer of Claim 1. Applicants respectfully submit that, in Figure 2A of Heim, vias 216 are not shown as being located below the outermost perimeter of pad metal layer 214. Referring to Figure 2A, instead of vias as contended in the outstanding Office Action, portions of inter-layer dielectric 210 actually lie below the outermost perimeter of pad metal layer 214. This

characterization of Heim is corroborated by Figure 2B of Heim which shows a dashed line that circumscribes the perimeter region of pad metal layer 214. Referring to Figure 2B, vias 216 are located far inside of the perimeter region of pad metal layer 214 that is circumscribed by the dashed line. Consequently, as alluded to above, The Heim reference fails to remedy the deficiencies of Tanaka with regard to Claim 1.

With regard to Claim 6, Applicants respectfully submit that nowhere in the Tanaka and Heim references is a semiconductor device that includes the above discussed limitation of Claim 1 and further includes the limitation "wherein a probing process is performed on said center area of said pad metal layer" as is set forth in Claim 6 taught or suggested. With regard to Claim 7, Applicants respectfully submit that nowhere in the Tanaka and Heim references is a semiconductor device that includes the above discussed limitation of Claim 1 and further includes the limitation "wherein a wire-bonding process is performed on said center area of said pad metal layer" as is set forth in Claim 7 taught or suggested. With regard to Claim 8, Applicants respectfully submit that nowhere in the Tanaka and Heim references is a semiconductor device that includes the above discussed limitation of Claim 1 and further includes the limitation "wherein said semiconductor device is an integrated chip" as is set forth in Claim 8 taught or suggested.

Because of deficiencies of Tanaka and Heim discussed above, Applicants respectfully submit that Tanaka in view of Heim does not provide an adequate basis for rejection of Claim 1 under 35 U.S.C. §103 and, as such, Claim 1 is allowable. Accordingly, the Applicants respectfully submit that Claims 3 and 6-8 dependent on Claim 1 are likewise allowable as being dependent on allowable base claims (at least).

CONCLUSION

For at least the above-presented reasons, it is respectfully submitted that all remaining claims are in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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